REMARKS

Claims 1-5 and 7-12 are presented for examination. All outstanding rejections under 35 U.S.C. § 103 have been withdrawn. However, the Examiner applied new grounds of rejection.

In particular, claims 1-5 and 7-12 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

First, the Examiner contends that the phrase "digital test data produced by converting analog test data output from the digital-to-analog converter circuit into a digital signal" in claims 1 and 7 is not clear. The Examiner notes that a digital-to-analog converter circuit outputs analog signals only.

However, the claim language does not indicate that the digital-to-analog converter circuit outputs a digital signal. Instead, claims 1 and 7 recite that digital test data are produced by converting the analog output of the digital-to-analog converter circuit into a digital signal.

Further, claim 1 recites that the data memory is divided into two memory sections such that, when digital test data is stored in one memory section, digital test data previously stored in the other memory section is loaded for analysis purpose. The Examiner contends that it is not clear from this language "how the memory sections are used for analysis purposes," and "if there could be a switch means to choose which section to use for analysis purposes."

It is well settled that the pivotal issue generated by a rejection under the second paragraph of 35 U.S.C. § 112 is whether one having ordinary skill in the art, with the supporting specification in hand, would be able to ascertain the scope of the claims with reasonable precision. ***In re Moore***, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971); ***In re Hammack***, 427 F.2d 1378, 166 USPQ 204 (CCPA 1970). It should be emphasized that unpatented claims are reasonably construed in light of the supporting specification. ***In re Okuzawa***, 537 F.2d 545, 190

USPQ 464 (CCPA 1976); ***In re Royka***, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Moreover, reasonable precision is all that is required. See, for example, ***U.S. v. Telectronics Inc.***, 857 F.2d 778, 8 USPQ2d 1217; ***Hybritech, Inc, v. Monoclonal Antiobodies, Inc.***, 802 F.2d 1367, 231 USPQ 81 (Fed. Cir. 1986); ***In re Kroekel***, 504 F.2d 1143, 183 USPQ 610 (CCPA 1974).

A decision on whether a claim is invalid under this section of the statute requires a determination of whether those skilled in the art would understand what is claimed when the claim is read in light of the specification, ***Seattle Box Co. v Industrial Crating & Packing***, 731 F.2d 381, 385, 221 U.S.P.Q. 568, 574 (Fed. Cir. 1984). Claim language is viewed not in a vacuum, but in light of the teachings of the prior art and of the application disclosure as it would be interpreted by one possessing the ordinary level of skill in the art. ***In re Johnson***, 558 F.2d 1008, 194 USPQ 187 (CCPA 1977); ***In re Moore, supra***.

With the above legal precedents in mind, Applicants respectfully point out that the Examiner does not explain why one having ordinary skill in the art, armed with the supporting specification, would have been confused as to the scope of claim 1 when read in light of the disclosure.

For example, FIG. 7 of the drawings and the specification on pages 14-17 disclose that data memory 66 is composed of first memory device 66A that constitutes memory bank A, and second memory device 66B that constitutes memory bank B. Switching between these two memory devices is controlled by using three connection changeover circuits 81, 83 and 85. For example, the first changeover circuit 83 provides interconnection between the memory banks A and B, and DSP analysis section 69 and ADC/DAC measurement section 23.

Accordingly, one having ordinary skill in the art, armed with the supporting specification and drawings, would understand what is claimed in claim 1.

It is believed that the claims fully comply with the statutory requirement to set out and circumscribe a subject matter area with a reasonable degree of precision and particularity. Therefore, Applicants respectfully submit that the rejection of the claims under 37 CFR 112, second paragraph, is improper and should be withdrawn.

Further, claims 1 and 7 have been rejected under the obviousness-type double patenting doctrine as being unpatentable over claims 1 and 10 of U.S. patent No. 6,642,736. This rejection is respectfully traversed for the following reasons.

It is well settled that any analysis employed in an obviousness-type double patenting rejection parallels the guidelines for analysis of a 35 U.S.C. § 103 obviousness determination. ***In re Braat,*** 937 F.2d 589, 19 USPQ2d 1289 (Fed. Cir. 1991). The test for obviousness under 35 U.S.C. § 103 is what the combined teachings of the references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of *prima facie* obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

The Examiner admits that the claims of the '736 patent do not recite that the data memory is divided into two memory sections, as claims 1 and 7 require. However, the Examiner takes the position that "it would be obvious of having two sections since the claim 1 of the patent recites "data memory to store the digital test outputs" and "analyzer portion to analyze each of said digital test outputs."

The Examiner's position is respectfully traversed. One skilled in the art of data processing would understand that it is not necessary to have two memory sections in order to

store digital test outputs and supply them to an analyzer. One memory section is sufficient to perform this function.

Moreover, the claims of the patent do not suggest that when digital test data is stored in one memory section, digital test data previously stored in the other memory section is loaded for analysis purpose, as claim 1 of the present patent application recites.

Further, the claims of the patent do not suggest storing first digital test data derived from the semiconductor integrated circuit in the first memory section while providing second digital test data derived from the semiconductor integrated circuit and data previously stored in the second memory section to an analysis device configured to analyze digital test data stored in the data memory, as claim 7 of the present patent application recites.

Accordingly, the claims of the patent are not sufficient to suggest the subject matter of claims 1 and 7 of the present patent application. Hence, the Examiner's rejection of claims 1 and 7 under the obviousness-type double patenting doctrine as being unpatentable over claims 1 and 10 of U.S. patent No. 6,642,736 is unwarranted and should be withdrawn.

In view of the foregoing, and in summary, claims 1-5 and 7-12 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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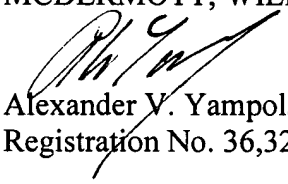

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